Amendments to the Drawings:

The attached sheets of drawings include new figures 54A, 54B, and 54C.

Attachment: Sheets Including New Figures.

REMARKS/ARGUMENTS

In the specification, new paragraph [0077.1] added after paragraph [0077] is taken from the appendix[1] at pages 261-63. In the specification, new paragraphs 0236.1 and 0236.2 added after paragraph 0236 are taken from the appendix at pages 261-63. The new paragraphs describe newly added figures.

In the drawings, new Figures 54A, 54B, and 54C added to the figures are taken from the appendix at pages 261-63.

Claims 1-22 remain unchanged. Claims 23-32 have been canceled, and new claims 33-52 have been added. Claims 12-32 are rejected under 35 U.S.C. 101 as allegedly being directed to non-statutory subject matter. Claims 1, 2, 4-13,15-24, and 26-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer (US Patent No. 6,823,353) in view of Kabir (US Patent No. 5,933,160). Claims 3, 14, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fischer and Kabir and further in view of Cohen (US Patent No. 5,751,614). Claims 1-22 and 33-52 are pending in this application.

Rejections under 35 U.S.C. § 101

Regarding the non-statuatory subject matter rejections, claims 12-22 are amended, and claims 23-32 are canceled. As amended, claims 12-22 are believed to overcome the non-statutory subject matter rejections. Support for this amendment can be found, for example, in paragraph [0079] of the published application.

Rejections under 35 U.S.C. § 103

Regarding the obviousness rejections, each of the two primary references, Fischer and Kabir, cited by the Examiner fail to qualify as prior art to the pending claims. The present application claims priority back to the 8/16/95 filing date of U.S. Patent Application No. 08/516,036, which issued into U.S. Patent No. 5,742,840 (the '840 patent). This chain of priority also includes a continuation-in-part application, U.S. Patent Application No. 09/382,402, which

[1] The appendix referred to here is part of the present application as filed. This appendix and is also submitted in one or more parent applications to the present application.

issued into U.S. Patent no. 6,295,599 (the '599 patent). The priority claim is hereby reproduced for the convenience of the Examiner:

> This application is a continuation of U.S. patent application Ser. No. 10/646,787, filed Aug. 25, 2003, which is a continuation of U.S. patent application Ser. No. 09/922,319, filed Aug. 2, 2001, which is a continuation of U.S. patent application Ser. No. 09/382,402, filed Aug. 24, 1999, now U.S. Pat. No. 6,295,599, which claims the benefit of priority to Provisional Application No. 60/097,635 filed Aug. 24, 1998, and is a continuation-in-part of U.S. patent application Ser. No. 09/169,963, filed Oct. 13, 1998, now U.S. Pat. No. 6,006,318, which is a continuation of U.S. patent application Ser. No. 08/754,827, filed Nov. 22, 1996 now U.S. Pat. No. 5,822,603, which is a divisional of U.S. patent application Ser. No. 08/516,036, filed Aug. 16, 1995 now U.S. Pat. No. 5,742,840.

Fischer fails to qualify as prior art against the pending claims. Fischer is a continuation of application Ser. No. 09/760,969, filed 1/16/01, which claims priority to a divisional application Ser. No. 08/905,506, filed 7/31/97, which claims priority to application Ser. No. 08/575,778, filed 12/20/95, which is a continuation-in-part of and claims priority to Ser. No. 08/523,211, filed 9/5/95. Thus, Fisher was filed after the 8/16/95 priority date . As such, Fischer fails to qualify as prior art against the pending claims.

Kabir also fails to qualify as prior art against the pending claims. Kabir is a continuation of parent application Ser. No. 09/289,783, filed 4/9/99, which is a continuation of application. 08/563,059, filed 11/27/95. Thus, Kabir was filed after the 8/16/95 priority date and fails to qualify as prior art against the pending claims, as well.

All of the rejections under § 103 rely on the two primary references, Fisher and Kabir, which fail to qualify as prior art against the present claims. As such, the rejection under § 103 cannot stand, and claims 1-32 are allowable over the cited references.

Support For Pending Claims 1-22

As mentioned above, the priority date of 8/16/95 of the present application is established through a claim of priority that includes the '840 patent and its appendix (the '840 appendix) and the '599 patent and its appendix (the '599 appendix). Support for pending claims 1-22 and 33-52 as found in the '840 patent, the '840 appendix, the '599 patent, and the '599 appendix is presented below.

Regarding claim 1, the recited method for processing data in a programmable processor comprising in part "decoding and executing instructions that instruct a computer system to perform operations" is described in the '599 patent at Fig. 1 and col. 4, lines 11-59, and in the '840 patent at Fig. 7 and col. 11, line 51 through col. 12, line15.

Regarding claim 1, the recited method for processing data in a programmable processor further comprising in part "at least some of the instructions including a group floating-point instruction operating on first and second registers partitioned into a plurality of floating point operands, the floating point operands having a defined precision and the defined precision being dynamically variable, having a defined result precision which is equal to the defined precision of the operands" is described in the '599 appendix at p. 258-60, and the '840 appendix at p. 129-31.

Regarding claim 1, the recited method for processing data in a programmable processor further comprising in part "at least some group floating-point instruction being a group floating-point multiply-and-add instruction, further operating on a third register partitioned into a plurality of floating-point operands, operable to multiply the plurality of floating-point operands in the first and second registers and add the plurality of floating-point operands in the third register, each producing a floating-point value to provide a plurality of floating-point values, each of the floating-point values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for receiving the plurality of floating point values" is described in the '599 appendix at p. 264-66, and the '840 appendix at p. 136-37.

Regarding claim 2, the recited claim feature "wherein at least some group floating-point instruction being at least one member of the collection consisting of group floating-point subtract, group floating-point add, and group floating-point multiply, operable to perform a subtract, add and multiply respectively on the plurality of floating-point operands in the first and second registers, each producing a floating-point value to provide a plurality of floating-point values, each of the floating-point values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for receiving the plurality of floating point value" is described in the '599 appendix at p. 258-60, and the '840 appendix at p. 129-31.

Regarding claim 2, the recited claim feature wherein "at least some group floating-point instruction being at least one member of the collection consisting of group floating-point set less, and group floating-point set greater or equal, operable to perform a set-less and set-greater-or-equal operation, respectively, on the plurality of floating-point operands in the first and second registers, each producing a value to provide a plurality of values, each of the values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for receiving the plurality of values, wherein the value is zero if the operation produces a false result, and wherein the value is an identity value if the operation produces a true result" is described in the '599 appendix at p. 176-78, and the '840 appendix at p. 132-35.

Regarding claim 2, the recited claim feature wherein "at least some of the instructions comprising performing data manipulations on multiple operands stored in partitioned fields of registers wherein the data manipulations comprise copying or rearranging operands" is described in the '599 appendix at p. 186 and 213-18, and the '840 patent at col. 5, lines 48-56.

Regarding claim 3, the recited claim feature "wherein the zero value and the identity value are values that construct a bit mask operable to select between alternate expressions using a bitwise Boolean operation" is described in the '599 appendix at p. 186, and the '840 appendix at p. 126-28.

Regarding claim 4, the recited claim feature "wherein the catenated result has a width of 128 bits" is described in the '599 appendix at p. 258-60, and the '840 appendix at p. 129-31.

Regarding claim 5, the recited claim feature "wherein the catenated result is provided to a register" is described in the '599 appendix at p. 258-60 and 264-66, and the '840 appendix at p. 129-31 and 136-37.

Regarding claim 6, the recited claim feature "wherein the defined precision is 16 bits" is described in the '599 appendix at p. 258-60 and 264-66, and the '840 appendix at p. 129-31 and 136-37.

Regarding claim 7, the recited claim feature "wherein the defined precision is a format comprising one sign bit, five exponent bits and ten significand bits" is described in the '599 appendix at p. 15, and the '840 patent at Fig. 9(b) and col. 15, lines 63-65.

Regarding claim 8, the recited claim feature "wherein the defined precision is 32 bits" is described in the '599 appendix at p. 258-60 and 264-66, and the '840 appendix at p. 129-31 and 136-37.

Regarding claim 9, the recited claim feature "wherein the precision of the group floating-point instructions is a format comprising one sign bit, eight exponent bits and 23 significand bits" is described in the '599 appendix at p. 16, and the '840 patent at Fig. 9(b) and col. 15, lines 63-65.

Regarding claim 10, the recited claim feature "wherein the defined precision is 64 bits" is described in the '599 appendix at p. 258-60 and 264-66, and the '840 appendix at p. 129-31 and 136-37.

Regarding claim 11, the recited claim feature "wherein the precision of the group floating-point instructions is a format comprising one sign bit, eleven exponent bits and 52 significant bits" is described in the '599 appendix at p. 16, and the '840 patent at Fig. 9(b) and col. 15, lines 63-65.

Regarding claim 12, the recited computer-readable medium having instructions in part "that instruct a computer system to perform operations" is described in the '599 patent at Fig. 1 and col. 4, lines 11-59, and in the '840 patent at Fig. 7 and col. 11, line 51 through col. 12, line15.

Regarding claim 12, the recited computer-readable medium further having instructions "at least some of the instructions including a group floating-point instruction operating on first and second registers partitioned into a plurality of floating point operands, the floating point operands having a defined precision and the defined precision being dynamically variable, having a defined result precision which is equal to the defined precision of the operands" is described in the '599 appendix at p. 258-60, and the '840 appendix at p. 129-31.

Regarding claim 12, the recited computer-readable medium further having instructions "at least some group floating-point instruction being a group floating-point multiply-and-add instruction, further operating on a third register partitioned into a plurality of floating-point operands, operable to multiply the plurality of floating-point operands in the first and second registers and add the plurality of floating-point operands in the third register, each producing a

floating-point value to provide a plurality of floating-point values, each of the floating-point values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for receiving the plurality of floating point values" is described in the '599 appendix at p. 264-66, and the '840 appendix at p. 136-37.

Regarding claim 13, the recited claim feature of having in part "at least some group floating-point instruction being at least one member of the collection consisting of group floating-point subtract, group floating-point add, and group floating-point multiply, operable to perform a subtract, add and multiply respectively on the plurality of floating-point operands in the first and second registers, each producing a floating-point value to provide a plurality of floating-point values, each of the floating-point values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for receiving the plurality of floating point values" is described in the '599 appendix at p. 258-60, and the '840 appendix at p. 129-31.

Regarding claim 13, the recited claim feature of having in part "at least some group floating-point instruction being at least one member of the collection consisting of group floating-point set less, and group floating-point set greater or equal, operable to perform a set-less and set-greater-or-equal operation, respectively, on the plurality of floating-point operands in the first and second registers, each producing a value to provide a plurality of values, each of the values capable of being represented by the defined result precision, and a catenated result having a plurality of partitioned fields for receiving the plurality of values, wherein the value is zero if the operation produces a false result, and wherein the value is an identity value if the operation produces a true result" is described in the '599 appendix at p. 176-78, and the '840 appendix at p. 132-35.

Regarding claim 13, the recited claim feature of having in part "at least some of the instructions comprising performing data manipulations on multiple operands stored in partitioned fields of registers wherein the data manipulations comprise copying or rearranging operands" is described in the '599 appendix at p. 186 and 213-18, and the '840 patent at col. 5, lines 48-56.

Regarding claim 14, the recited claim feature "wherein the zero value and the identity value are values that construct a bit mask operable to select between alternate expressions using

a bitwise Boolean operation" is described in the '599 appendix at p. 186, and the '840 appendix at p. 126-28.

Regarding claim 15, the recited claim feature "wherein the catenated result has a width of 128 bits" is described in the '599 appendix at p. 258-60, and the '840 appendix at p. 129-31.

Regarding claim 16, the recited claim feature "wherein the catenated result is provided to a register" is described in the '599 appendix at p. 258-60 and 264-66, and the '840 appendix at p. 129-31 and 136-37.

Regarding claim 17, the recited claim feature "wherein the defined precision is 16 bits" is described in the '599 appendix at p. 258-60 and 264-66, and the '840 appendix at p. 129-31 and 136-37.

Regarding claim 18, the recited claim feature "wherein the defined precision is a format comprising one sign bit, five exponent bits and ten significand bits" is described in the '599 appendix at p. 15, and the '840 patent at Fig. 9(b) and col. 15, lines 63-65.

Regarding claim 19, the recited claim feature "wherein the defined precision is 32 bits" is described in the '599 appendix at p. 258-60 and 264-66, and the '840 appendix at p. 129-31 and 136-37.

Regarding claim 20, the recited claim feature "wherein the precision of the group floating-point instructions is a format comprising one sign bit, eight exponent bits and 23 significand bits" is described in the '599 appendix at p. 16, and the '840 patent at Fig. 9(b) and col. 15, lines 63-65.

Regarding claim 21, the recited claim feature "wherein the defined precision is 64 bits" is described in the '599 appendix at p. 258-60 and 264-66, and the '840 appendix at p. 129-31 and 136-37.

Regarding claim 22, the recited claim feature "wherein the precision of the group floating-point instructions is a format comprising one sign bit, eleven exponent bits and 52 significand bits" is described in the '599 appendix at p. 16, and the '840 patent at Fig. 9(b) and col. 15, lines 63-65.

Support for New Claims 33-52

New claims 33-52 are fully supported by the present specification. Support for specific claim elements is identified below by citing to the present specification as published (United States Patent Publication Number US2004/0205324).

Regarding claim 33, the recited method for performing data operations in a programmable processor comprising in part "executing a plurality of instructions each of which (i) operates on data stored in a first, a second and a third register, the data in the first register comprising a first plurality of equal-sized data elements, the data in the second register comprising a second plurality of equal-sized data elements, the data in the third register comprising a third plurality of equal-sized data elements, (ii) multiplies each data element in the first register with a corresponding data element in the second register to produce a plurality of products, and (iii) adds each product in the plurality of products to a corresponding data element in the third register to produce a plurality of sums, and (iv) provides the plurality of sums as a catenated result; wherein the plurality of instructions includes a floating-point instruction that operates on floating-point data elements stored in the first, second and third registers" is described at Figures 38D-F and paragraphs 0238-0239.

Regarding claim 34, the recited claim feature "wherein each of the plurality of instructions includes a field that indicates the size of each of the first plurality and second plurality of data elements" is described at Figures 38D-F and paragraphs 0238-0239.

Regarding claim 35, the recited claim feature "wherein the catenated result is returned to a fourth register" is described at Figures 38D-F and paragraphs 0238-0239.

Regarding claim 36, the recited claim feature "wherein for the floating-point instruction, each of the first plurality and second plurality of equal-sized data elements is a floating-point value that is n bits wide, and each of the third plurality of equal-sized data elements is also a floating-point value that is n bits wide" is described at Figures 38D-F and paragraphs 0238-0239.

Regarding claim 37, the recited claim feature "wherein the floating-point instruction multiplies data elements of 32-bit floating-point data and adds data elements of 32-bit floating-point data" is described at Figures 38D-F and paragraphs 0238-0239.

Regarding claim 38, the recited claim feature "wherein the plurality of instructions includes an integer instruction that operates on integer data elements stored in the first, second and third registers" is described at Figures 54A-C, and paragraph 0236.1.

Regarding claim 39, the recited claim feature "wherein for the integer instruction, each of the first plurality and second plurality of equal-sized data elements is an integer value that is n bits wide, and each of the third plurality of equal-sized data elements is an integer value that is 2*n bits wide" is described at Figures 54A-C, and paragraph 0236.1.

Regarding claim 40, the recited claim feature "wherein the integer instruction multiplies data elements of 8-bit integer data and adds data elements of 16-bit integer data" is described at Figures 54A-C, and paragraph 0236.1.

Regarding claim 41, the recited claim feature "wherein the integer instruction multiplies data elements of 16-bit integer data and adds data elements of 32-bit integer data" is described at Figures 54A-C, and paragraph 0236.1.

Regarding claim 42, the recited claim feature "wherein the integer instruction multiplies data elements of 32-bit integer data and adds data elements of 64-bit integer data" is described at Figures 54A-C, and paragraph 0236.1.

Regarding claim 43, the recited computer-readable storage medium having stored therein "instructions that cause a computer processor to perform operations on data stored in registers in the computer processor" is described at Figures 38D-F and paragraphs 0238-0239.

Regarding claim 43, the recited instructions stored in the computer-readable storage medium further comprising in part "a plurality of instructions each of which (i) operates on data stored in a first, a second and a third register, the data in the first register comprising a first plurality of equal-sized data elements, the data in the second register comprising a second plurality of equal-sized data elements, the data in the third register comprising a third plurality of equal-sized data elements, (ii) multiplies each data element in the first register with a corresponding data element in the second register to produce a plurality of products, and (iii) adds each product in the plurality of products to a corresponding data element in the third register to produce a plurality of sums, and (iv) provides the plurality of sums as a catenated result; wherein the plurality of instructions includes a floating-point instruction that operates on

floating-point data elements stored in the first, second and third registers" is described at Figures 38D-F and paragraphs 0238-0239.

Regarding claim 44, the recited claim feature "wherein each of the plurality of instructions includes a field that indicates the size of each of the first plurality and second plurality of data elements" is described at Figures 38D-F and paragraphs 0238-0239.

Regarding claim 45, the recited claim feature "wherein the catenated result is returned to a fourth register" is described at Figures 38D-F and paragraphs 0238-0239.

Regarding claim 46, the recited claim feature "wherein for the floating-point instruction, each of the first plurality and second plurality of equal-sized data elements is a floating-point value that is n bits wide, and each of the third plurality of equal-sized data elements is also a floating-point value that is n bits wide" is described at Figures 38D-F and paragraphs 0238-0239.

Regarding claim 47, the recited claim feature "wherein the floating-point instruction multiplies data elements of 32-bit floating-point data and adds data elements of 32-bit floating-point data" is described at Figures 38D-F and paragraphs 0238-0239.

Regarding claim 48, the recited claim feature "wherein the plurality of instructions includes an integer instruction that operates on integer data elements stored in the first, second and third registers" is described at Figures 54A-C, and paragraph 0236.1.

Regarding claim 49, the recited claim feature "wherein for the integer instruction, each of the first plurality and second plurality of equal-sized data elements is an integer value that is n bits wide, and each of the third plurality of equal-sized data elements is an integer value that is 2*n bits wide" is described at Figures 54A-C, and paragraph 0236.1.

Regarding claim 50, the recited claim feature "wherein the integer instruction multiplies data elements of 8-bit integer data and adds data elements of 16-bit integer data" is described at Figures 54A-C, and paragraph 0236.1.

Regarding claim 51, the recited claim feature "wherein the integer instruction multiplies data elements of 16-bit integer data and adds data elements of 32-bit integer data" is described at Figures 54A-C, and paragraph 0236.1.

Regarding claim 52, the recited claim feature "wherein the integer instruction multiplies data elements of 32-bit integer data and adds data elements of 64-bit integer data" is described at Figures 54A-C, and paragraph 0236.1.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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